35 U.S.C. § 103(a) as being unpatentable over the Saito et al. reference in view of the Araki reference and further in view of the Hsueh et al. reference.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

An exemplary embodiment of the claimed invention, as defined by, for example, independent claim 11, is directed to a method for fabricating a semiconductor device. The method includes depositing a metallic conductive film on an underlying insulating film, depositing a first insulator film on the metallic conductive film, depositing a second insulator film on the first insulator film, patterning the first and second insulator films, etching the second insulator film to have a patterned area that is smaller than the first insulator film, and patterning the metallic conductive film.

Conventional methods for fabricating semiconductor devices have problems with defects such as a void and/or a short-circuit.

For example, in a first conventional method a two-layer mask is used to pattern a bit line. However, the use of a two-layer mask tends to increase the depth of sidewall films and, therefore, increases the aspect ratio between the depth of the sidewall films and the space between the sidewall films. This increased aspect ratio increases the likelihood that a defect, such as a void, is formed in an interlayer dielectric film. (Page 3, line 2 - 10).

In a second conventional method, a single-layer mask may be used to pattern a bit line. The use of a single-layer mask provides a reduced thickness in comparison to a two-layer mask and generally reduces the likelihood of forming a defect, such as a void, in an interlayer dielectric film. However, this reduction in thickness may result in an exposure of

the bit lines when a contact hole is formed. This may result in a short-circuit defect. (Page 4, lines 3-23).

In summary, a two-layer hard mask may cause a defect in the embedding structure due to the increased aspect ratio, while a single-layer hard mask may cause a short circuit failure. (Page 5, lines 2-10).

In stark contrast, the present invention solves these problems by etching the second insulator film to have a patterned area that is smaller than the first insulator film. In this manner, the present invention reduces the likelihood of a short circuit failure while enabling the use of a two-layer mask. (Page 6, lines 1 - 6).

II. THE PRIOR ART REJECTIONS

A. The Saito et al. reference in view of the Araki reference

Regarding the rejection of claims 11-23 and 26, the Examiner alleges that the Araki reference would have been combined with the Saito et al. reference to form the claimed invention.

However, as explained during the personal interview on February 9, 2005, Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

As agreed by Examiner Novacek during the personal interview, none of the applied references teaches or suggests the features of the present invention including etching the second insulator film to have a patterned area that is smaller than the first insulator film as recited by independent claim 11. As explained above, this feature is important for reducing the likelihood of a short circuit failure while enabling the use of a two-layer mask.

Indeed, the Examiner does not present a *prima facie* case for obviousness because the Examiner does not allege that any of the applied references teaches or suggests anything at all that is even remotely related to a patterned area, let alone etching the second insulator film to have a patterned area that is smaller than the first insulator film.

Indeed, the Office Action admits that the Saito et al. reference does not teach or suggest this feature. The Office Action then attempts to rely upon the disclosure in the Araki reference to remedy the deficiencies of the Saito et. al. reference.

In particular, the Office Action alleges that the Araki reference "teaches that it is beneficial to etch the top (cap) layer on the metallic lines to narrow its width."

However, the Examiner does not allege that the Araki reference teaches anything at all regarding a patterned area, let alone etching the second insulator film to have a patterned area that is smaller than the first insulator film.

In stark contrast to the present invention, the Araki reference discloses rounding the corners of the cap layer.

In particular, the Araki reference teaches that "the angle of said oxide film by which patterning was carried out, and (sic) is made round. . . . In case said oxide film is etched, the angle of an oxide film is dropped and it is made round." (Emphasis added, [0006]) "A part for the corner of the mask oxide film 105 upper part fails to be diminished by sputter etching, and etching section 105a with the round upper part is formed." (Emphasis added, [0012]). In other words, the Araki reference clearly discloses that the "angles" (i.e. upper corners) of the oxide film 105 is "diminished" (i.e. rounded) until the oxide film 105 has a "round upper part."

The Araki reference does not teach or suggest that the oxide film 105 has a smaller

patterned area. Indeed, the patterned area of the oxide film 105 clearly is not smaller at all. Rather, only the upper corners or the oxide film 105 are rounded to form a round upper part.

Indeed, the Araki reference does not disclose any layer having a smaller patterned area, let alone a second insulating layer having a smaller patterned area than a first insulating layer.

As explained above, the Araki reference merely discloses rounding the upper corners of an oxide film 105 to form a round upper part. The Araki reference does not teach or suggest anything at all about etching the oxide film 105 to reduce the patterned area, let alone to reduce the patterned area so that it is smaller than another insulator film.

Further, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different and unrelated matters and problems.

Specifically, the Saito et al. reference is directed to providing a technique for exposing semiconductor regions over the surface of a semiconductor substrate in self-alignment wiring lines which provides a lower aspect ratio for the connection holes and which prevents separation or bulging of a cap insulating film. (Col. 1, lines 8-11 and col. 3, lines 40-45).

In stark contrast, the Araki reference is concerned with the completely different and unrelated problem preventing deterioration of film coverage at the time of forming an interlayer film. (See: PROBLEM TO BE SOLVED).

One of ordinary skill in the art who was concerned with lowering aspect ratio for connection holes and preventing separation or bulging of a cap insulating film as the Saito et al. reference is concerned with addressing would not have referred to the Araki reference, and vice-versa, because the Araki reference is concerned with the completely different and

unrelated problem of preventing deterioration of film coverage at the time of forming an interlayer film. Thus, the references would not have been combined.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 11-23 and 26.

B. The Saito et al. reference in view of the Araki reference and in further view of the Hsueh et al. reference.

Regarding the rejection of claim 29, the Examiner alleges that the Araki reference would have been combined with the Saito et al. reference and further alleges that the Hsueh et al. reference would have been combined with a combination of the Araki reference and the Saito et al. reference to form the claimed invention.

Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

None of the applied references teaches or suggests the features of the present invention including etching the second insulator film to have a patterned area that is smaller than the first insulator film as recited by independent claim 11 from which claim 29 depends. As explained above, this feature is important for reducing the likelihood of a short circuit failure while enabling the use of a two-layer mask.

Indeed, the Examiner again fails to present a *prima facie* case for obviousness because the Examiner does not allege that any of the applied references teaches or suggests anything at all that is even remotely related to a patterned area, let alone etching the second insulator film to have a patterned area that is smaller than the first insulator film

As explained above, neither of the Saito et al. reference and the Araki reference teaches or suggests the features of the claimed invention including etching the second insulator film to have a patterned area that is smaller than the first insulator film as recited by independent claim 11.

The Hsueh et al. reference does not remedy the deficiencies of the Saito et al. reference and the Araki reference.

Again, the Examiner does not allege that the Hsueh et al. reference teaches or suggests etching the second insulator film to have a patterned area that is smaller than the first insulator film as recited by independent claim 11.

Further, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different and unrelated matters and problems.

As explained above, the Saito et al. reference and the Araki reference would not have been combined because they are directed to completely different and unrelated matters and problems.

In contrast to the Saito et al. reference and the Araki reference, the Hsueh et al. reference is directed to the completely different and unrelated problem of sharp corners at the isolation edge where the silicon substrate and oxide intercept in shallow trench isolation elements. (Col. 1, lines 10 - 18).

One of ordinary skill in the art who was concerned with lowering aspect ratio for connection holes and preventing separation or bulging of a cap insulating film as the Saito et al. reference is concerned with addressing or who was concerned with the problem of preventing deterioration of film coverage at the time of forming an interlayer film as the

Araki reference is concerned would not have referred to the Hsueh et al. reference, and vice-versa, because the Hsueh et al. reference is concerned with the completely different and unrelated problem of sharp corners at the isolation edge where the silicon substrate and oxide intercept in shallow trench isolation elements. Thus, the references would not have been combined.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claim 29.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-29, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 7/28/05

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Request for Reconsideration by facsimile with the United States Patent and Trademark Office to Examiner Christy L. Novacek, Group Art Unit 2822 at fax number (571) 273-8300 this 28th day of July, 2005.

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